CLAIMS

What is claimed is:

1. A method for treating a gate structure comprising a high-K gate dielectric stack to improve electric performance characteristics comprising the steps of:

providing a gate dielectric layer stack comprising a binary oxide over a silicon substrate;

forming a polysilicon layer over the gate dielectric layer stack;

lithographically patterning and etching to form a gate structure; and,

carrying out at least one plasma treatment of the gate structure comprising a plasma source gas selected from the group consisting of H_2, N_2, O_2, and NH_3.

2. The method of claim 1, further comprising the step of annealing the gate structure following the at least one plasma treatment.

3. The method of claim 2, wherein the step of annealing comprises a temperature of from about 600 °C to about 750 °C.

4. The method of claim 2, wherein the step of annealing comprises an ambient consisting essentially of nitrogen.

5. The method of claim 1, wherein the gate dielectric layer stack comprises a lowermost SiO_2 layer formed over the silicon substrate.

6. The method of claim 1, wherein the gate dielectric layer stack comprises a high-K material selected from the group consisting of tantalum oxides, titanium oxides,, hafnium oxides, yttrium oxides, lanthanum oxides, zirconium oxides , and silicates and aluminates thereof.

7. The method of claim 1, wherein the dielectric layer stack consists essentially of a lowermost SiO_2 layer and an overlying hafnium oxide layer.

8. The method of claim 7, wherein the hafnium oxide layer is formed according to an ALCVD method at a temperature of less than about 300 °C.

9. The method of claim 1, wherein the plasma source gas is selected from the group consisting of hydrogen and nitrogen.

10. The method of claim 1, wherein the plasma treatment is carried out for a period of between about 10 minutes and about 90 minutes.

11. The method of claim 1, wherein the plasma treatment is carried out at a pressure of between about 100 mTorr and about 10 Torr.

12. The method of claim 11, wherein the plasma treatment is carried out at a pressure of between about 100 mTorr and about 5 Torr.

13. A method for treating a gate structure comprising a high-K gate dielectric stack to improve flatband Voltage and threshold Voltage characteristics of a CMOS device comprising the steps of:

providing a gate dielectric layer stack comprising at least one high-K dielectric having a dielectric constant greater than about 10 over a silicon substrate;

forming a polysilicon layer over the gate dielectric layer stack;

lithographically patterning and etching to form a gate structure;

carrying out at least one plasma treatment of the gate structure comprising a plasma source gas selected from the group consisting of H_2, N_2, O_2, and NH_3; and,

annealing the gate structure following the at least one plasma treatment.

14. The method of claim 13, wherein the step of annealing comprises a temperature of from about 600 °C to about 750 °C.

15. The method of claim 14, wherein the step of annealing comprises an ambient selected from the group consisting of H_2, N_2, O_2, and NH_3.

16. The method of claim 13, wherein the gate dielectric layer stack comprises a lowermost SiO_2 layer formed over the silicon substrate.

17. The method of claim 13, wherein the high-K dielectric is selected from the group consisting of tantalum oxides, titanium oxides,, hafnium oxides, yttrium oxides, lanthanum oxides, zirconium oxides , and silicates and aluminates thereof.

18. The method of claim 13, wherein the gate dielectric layer stack consists essentially of a lowermost SiO_2 layer and an overlying hafnium oxide layer.

19. The method of claim 13, wherein the plasma source gas consists essentially of hydrogen (H_2).

20. The method of claim 13, wherein the plasma treatment is carried out at a pressure of between about 100 mTorr and about 5 Torr.